IN THE CLAIMS

1. (Previously Amended) A semiconductor integrated circuit device comprising:

a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;

a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage;

a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

2. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection circuit comprises

a first reset element responsive to activation of said first power-on detection signal for resetting a first node to a first voltage level,

a second reset element responsive to activation of said second power-on detection signal for resetting said first node to said first voltage level, and

a circuit coupled to said first node and receiving said first power supply voltage as an operation power supply voltage for inactivating said main power-on detection signal and setting said first node to a second voltage level when both of said first and second power-on detection signals are inactivated.

3. (Original) The semiconductor integrated circuit device according to claim 1, further comprising a converting voltage application detection circuit receiving a voltage different in voltage level from said second power supply voltage as an operation power supply voltage for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal.

4. (Original) The semiconductor integrated circuit device according to claim 1, further comprising:

an internal voltage generation circuit for generating an internal voltage from said first power supply voltage, said internal voltage differing in voltage level from said second power supply voltage; and

an internal circuit reset when said main power-on detection signal is activated, and activated, when said main power-on detection signal is inactivated, for converting a signal having an amplitude of said second power supply voltage level into a signal having an amplitude of the internal voltage level.

5. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a boosted voltage higher in voltage level than said first power supply voltage.

6. (Original) The semiconductor integrated circuit device according to claim 4, wherein said internal voltage is a down-converted voltage lower in voltage level than said first power supply voltage.

7. (Original) The semiconductor integrated circuit device according to claim 1, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, the storage device and the logic circuit being integrated on a common semiconductor chip.

8. (Original) The semiconductor integrated circuit device according to claim 1, wherein said main power-on detection signal has an amplitude of the first power supply voltage level, and

said semiconductor integrated circuit device further comprises:

an internal voltage generation circuit for generating, from said first power supply voltage, an internal voltage different in voltage level from said second power supply voltage;

an internal signal generation circuit for generating an internal signal having an amplitude of the internal voltage level from a signal having an amplitude of the second power supply voltage level, said internal signal generation circuit including a buffer circuit receiving said internal voltage as an operation power supply voltage for generating said internal signal; and

a converting voltage application detection circuit for converting said main power-on detection signal into a converted voltage application detection signal having an amplitude of said internal voltage level and applying the converted voltage application detection signal to said buffer circuit, said buffer circuit being reset when said converted voltage application detection signal is activated.

9. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first power supply voltage to generate said internal voltage.

10. (Original) The semiconductor integrated circuit device according to claim 8, wherein said internal voltage generation circuit includes an internal down-converting circuit for down-converting said first power supply voltage to generate an internal power supply voltage as said internal voltage.

11. (Previously Amended) A semiconductor integrated circuit device comprising;

an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal

according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the second power supply voltage; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of the internal voltage power-up detection signal and the power-on detection signal.

12. (Original) The semiconductor integrated circuit device according to claim 11, further comprising an internal signal generation circuit inactivated when the main power-on detection signal from said main power-on detection circuit is activated, and activated, when said main power-on detection signal is inactivated, for generating an internal signal having an amplitude of said internal voltage level from a signal having an amplitude of said second power supply voltage level.

13. (Original) The semiconductor integrated circuit device according to claim 12, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal voltage as an operation power supply voltage and generating said internal signal, said buffer circuit being reset when said main power-on detection signal is activated and buffering a level converted signal to generate said internal signal when said main power-on detection signal is inactivated.

14. (Original) The semiconductor integrated circuit device according to claim 11, wherein said main power-on detection signal is a signal having an amplitude of said internal voltage level, and

said integrated circuit device further comprises

a level conversion circuit for converting a voltage level of said main power-on detection signal to generate a converted voltage application detection signal, and

an internal signal generation circuit inactivated when said converted voltage application detection signal is activated and activated, when said converted voltage application detection signal is inactivated, for converting a level of a signal having an amplitude of said second power supply voltage level to generate an internal signal having an amplitude equal to an amplitude of said converted voltage application detection signal.

15. (Original) The semiconductor integrated circuit device according to claim 14, further comprising an internal power supply circuit for generating, from said first power supply voltage, an internal power supply voltage different in voltage level from said internal voltage, wherein

said internal signal generation circuit includes a buffer circuit receiving said internal power supply voltage as an operation power supply voltage and buffering a level converted signal for outputting, said buffer circuit having an internal node being reset when said converted voltage application detection signal is activated.

16. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a boosting circuit for boosting said first power supply voltage.

17. (Original) The semiconductor integrated circuit device according to claim 11, wherein said internal voltage generation circuit includes a down-converting circuit for down-converting said first power supply voltage to generate said first internal voltage.

18. (Original) The semiconductor integrated circuit device according to claim 11, wherein the first and second power supply voltages are applied to a storage device and said second power supply voltage is applied to a logic circuit, said storage device and said logic circuit being integrated on a common semiconductor chip.

19. (Previously Amended) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages, each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage; and

a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up

detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (Previously Amended) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltages differing in voltage level from each other;

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage, to generate at least one power-on detection signal for the respective at least one power source voltage, said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage; and

main power-on detection circuitry responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last

activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.

21. (Previously Added) The semiconductor integrated device according to claim 1, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

22. (Previously Added) The semiconductor integrated circuit device according to claim 11, wherein activation of the detection signal indicates instability of a corresponding power supply voltage, and inactivation of the detection signal indicates stability of the corresponding power supply voltage.

23. (Previously Added) The semiconductor device according to claim 19, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

24. (Previously Added) The semiconductor device according to claim 20, wherein the activation of the detection signal indicates instability of a corresponding voltage and the inactivation of the detection signal indicates stability of the corresponding voltage.